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1 Cache Memories

Alan Jay Smith

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

2 The Kyushu University reconfigurable parallel processor: design of memory and intercommunicaiton architectures

Kazuaki Murakami, Shin-ichiro Mori, Akira Fukuda, Toshinori Sueyoshi, Shinji Tomita

June 1986 **Proceedings of the 3rd international conference on Supercomputing**

Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, citings, index terms

The reconfigurable parallel processor system under development at Kyushu University is an MIMD-type multiprocessor which consists of N processing-elements (currently N is 128) fully connected by S N × N crossbar networks (currently S is 1). Each PE (Processing Element) employs a Fujitsu SPARC MB86900/10 chip-set, a Weitek WTL1164/65 chip-set, an MMU (Memory Management Unit) with 64K b ...

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